SPECIFICATION AS AMENDED

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Referring to FIG. 3, showing static memory cell 5, containing gates 13 and 13', FIG. ~~2~~ 3(b) shows memory cell 5 in the latched condition. FIG. ~~2~~ 3(c) shows memory cell 5 in the blocking (not latched) condition. These conditions reflect CMOS latch-up action, initiated by gate voltage from gates 13 and 13'. Gates 13 and 13' induce latch-up in the gated lateral bipolar transistor device 10, thus creating one of the two bistable states for the static memory cell, as discussed in detail below.